Index- Computer Organization and Architecture

Common Data for Q1 Q2 and Q3 is given below

Consider a machine a 2-way set associative data cache of size 64 kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addressed and the page size is 4 Kbytes. A program to be run on this machine begins as follows.

```
double APR[1024] [1024]
int i,j;
/* initalize array APR to 0.0*/
for [i=0; i <1024 ; i ++)
for (j=0; k <1024;j++
ARR [i][j]=0.0;
```

The size of double 8 bytes. Array APR is in memory starting at the beginning of virtual page 0 x FF000 and
stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array APR..

1) The total size of the tags in the cache directory is

2 Marks GATE-CSE/IT-2008,GATE-CSE/IT-2008,GATE-CSE/IT-2008,GATE-CSE/IT-2008( )

[A] 32kbits [B] 34kbits
[C]64kbits [D]68kbits

2) Which of the following array elements has the same cache index as APR[0] [0]?

2 Marks GATE-CSE/IT-2008( )

[A] APR[0] [4] [B]APR[4] [0]
[C]ARR[0][5] [D]APR[5][0]

3) The cache hit ratio for this initialization loop is

2 Marks GATE-CSE/IT-2008,GATE-CSE/IT-2008( )

[A] 0% [B] 25%
[C]50% [D]75%

Common Data for Q4 and Q5 is given below

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system.
A 50 x 50 two-dimensional array of bytes is stored in the main memory starting from memory location 1100 H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

4) How many data cache misses will occur in total ?

2 Marks GATE-CSE/IT-2007( )

[A] 40 [B] 50
[C]56 [D]59

5) Which of the following lines of the data cache will be replaced by new blocks in accessing the array

2 Marks GATE-CSE/IT-2007,GATE-CSE/IT-2007( )

[A] line 4 to line 11 [B] line 4 to line 12
[C]line 0 to line 7 [D]line 0 to line 8

Common Data for Q7 and Q6 is given below

A CPU has a 32 KB direct mapped cache with 128-byte block size. Suppose A is a two dimensional array of size 512 x 512 with elements that occupy 8-bytes each/ Consider the following two C code segments, P1 and P2.

```
P1 : for(i=0;i<512;i++)              {
     for(j=0;j<512;j++)                    {
                x+ = A[i] [j];
        }
}
P2: for (i=0; i<512; i++)            {
          for(j=0 ; j<512 ; j++)   {
         {x + = A[j] [i];}
        }
}
```

P1 and P2 are executed independently with the same initial state, namely, the array A is not in the cache and i,j, x are in registers.

Let the number of cache misses experienced by P1 be M_1 and that for P2 be M_2.

6) The value of M_1 is

2 Marks GATE-CSE/IT-2006( )

[A] 0 [B] 2048

[C] 16384 [D] 262144

7) The value of the ratio M_1 / M_2 is

2 Marks GATE-CSE/IT-2006,GATE-CSE/IT-2006( )

[A] 0 [B] 1/16

[C] 1/8 [D] 16

Common Data for Q8 and Q9 is given below

Consider two cache organizations : The first one is 32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases A 2-to 1 multiplexer has latency of 0.6ns while a k-bit comparator has a latency of k/10-ns. The hit latency of the set associative organization is h_1 while that of the direct mapped one is h_2.

8) The value of h1 is

2 Marks GATE-CSE/IT-2006,GATE-CSE/IT-2006( )

[A] 2.4ns [B] 2.3ns

[C] 1.8ns [D] 1.7ns

9) The value of h_2 is

2 Marks GATE-CSE/IT-2006( )

[A] 2.4ns [B] 2.3ns

[C] 1.8ns [D] 1.7ns

Common Data for Q10 and Q11 is given below

Consider two cache organizations : The first one is 32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases A 2-to 1 multiplexer has latency of 0.6ns while a k-bit comparator has a latency of k/1-ns. The hit latency of the set associative organization is h1 while that of the direct mapped one is h2.

10) The value of h1 is

2 Marks GATE-CSE/IT-2006( )

[A] 2.4ns [B] 2.3ns

[C] 1.8ns [D] 1.7ns

11) The value of h2 is

2 Marks GATE-CSE/IT-2006( )

[A] 2.4ns [B] 2.3ns

[C] 1.8ns [D] 1.7ns

12) Consider a small two-way set-associative cache memory, consitsting of four blocks. For choosing the block to be replace, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12, 0, 12, 8

2 Marks GATE-CSE/IT-2004( )

[A] 2 [B] 3
[C] 4 [D] 5

13) Increasing the RAM of a computer typically improves performance because

1 Marks GATE-CSE/IT-2005( )

[A] Virtual memory increases [B] Larger RAMs are faster
[C] Fewer page faults occur [D] Fewer segmentation faults occur

14) Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively.

2 Marks GATE-CSE/IT-2005( )

[A] 10,17 [B] 10,22
[C] 15,17 [D] 5,17

15) A CPU has a cache with block size 64 bytes. The main memory has k banks, each bank being c bytes wide. Consecutive c-byte chunks are mapped on consecutive banks with warp-around. All the k banks can be accessed in parallel, but two accesses to the same bank must be serialized. A cache block access ay involve multiple iterations of parallel bank accesses depending on the amount of data obtained by accessing all the k banks in parallel. Each iteration requires decoding the bank numbers to be accessed in parallel and this takes k/2 ns. The latency of one bank access is 80 ns. If c=2 and k=24, then latency of retrieving a cache block starting at address zero from main memory is

2 Marks GATE-CSE/IT-2006( )

[A] 92ns [B] 104ns
[C] 172ns [D] 184ns

16) Consider a small two-way set-associative cache memory, consitsting of four blocks. For choosing the block to be replace, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12, 0, 12, 8

2 Marks GATE-CSE/IT-2004( )

[A] 2 [B] 3
[C] 4 [D] 5

17) Increasing the RAM of a computer typically improves performance because

1 Marks GATE-CSE/IT-2005( )

[A] Virtual memory increases [B] Larger RAMs are faster
[C] Fewer page faults occur [D] Fewer segmentation faults occur

18) Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively.

2 Marks GATE-CSE/IT-2005( )

[A] 10,17 [B] 10,22
[C] 15,17 [D] 5,17

19) A CPU has a cache with block size 64 bytes. The main memory has k banks, each bank being c bytes wide. Consecutive c-byte chunks are mapped on consecutive banks with warp-around. All the k banks can be accessed in parallel, but two accesses to the same bank must be serialized. A cache block access ay involve multiple interations of parallel bank accesses depending on the amount of data obtained by accessing all the k banks in parallel. Each iteration requires decoding the bank numbers to be accessed in parallel and this takes k/2 ns. The latency of one bank access is 80 ns. If c=2 and k=24, then latency of retrieving a cache block starting at address zero from main memory is

2 Marks GATE-CSE/IT-2006( )

[A] 92ns [B] 104ns
[C] 172 ns [D] 184 ns

20) Consider 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively

1 Marks GATE-CSE/IT-2007( )

[A] 9,6,5 [B] 7,7,6
[C] 7,5,8 [D] 9,5,6

21) For inclusion to hold between two cache level L1 and L2 in a multilevel cache hierarchy, which of the following
are necessary ?
1. L1 must be a write-through cache
2. L2 must be write-through cache
3. The associativity of L2 must be greater that of L1
4. The L2 cache must be at least as large as the L1 cache.

2 Marks GATE-CSE/IT-2008( )

[A] 4 only
[B] and 2 only
[C] 1,2 and 4 only
[D] 1,2,3 and 4

22) How many 32K x 1 RAM chips are needed to provide a memory capacity of 256 K-bytes ?

1 Marks GATE-CSE/IT-2009( )

[A] 8
[B] 32
[C] 64
[D] 128

23) How many 32K x 1 RAM chips are needed to provide a memory capacity of 256 K-bytes ?

1 Marks GATE-CSE/IT-2008( )

[A] 8
[B] 32
[C] 64
[D] 128

24) Consider a 4 way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order :
0,255, 1,4,3,8,133, 159, 216, 129, 63, 8,48,32,73, 92, 155
Which one of the following memory block will NOT be in cache if LRU replacement policy is used ?

2 Marks GATE-CSE/IT-2009( )

[A] 3
[B] 8
[C] 129
[D] 216

25) The main memory of a computer has 2 cm blocks while the cache has 2 c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set

1 Marks GATE-CSE/IT-1999( )

[A] (k mod m) of the cache
[B] (k mod c) of the cache
[C] (k mod 2c) of the cache
[D] (k mod 2 cm) of the cache

26) Which of the following devices should get higher priority in assigning interrupts?

1 Marks GATE-CSE/IT-1998( )

[A] Hard disk
[B] Printer
[C] keyboard
[D] Floppy disk

27) Locality of reference implies that the page reference being made by a process

1 Marks GATE-CSE/IT-1997( )

[A] will always be to the page used in the previous page reference
[B] is likely to be to one of the pages used in the last few page references
[C] will always be to one of the pages existing in memory
[D] will always lead to a page fault

28) A ROM is sued to store the table for multiplication of two 8-bit unsigned integers. The size of ROM required is

1 Marks GATE-CSE/IT-1996( )

[A] 256 * 16
[B] 64 k * 8
[C] 4k * 16
[D] 64k * 16

29) Both's algorithm for integer multiplication gives worst performance when the multiplier pattern is

1 Marks GATE-CSE/IT-1996( )

[A] 101010 1010
[B] 100000 0001
[C] 111111 1111
[D] 011111 1110

30) The principle of locality justifies the use of

1 Marks GATE-CSE/IT-1995( )

[A] interrupts
[B] DMA
[C] polling
[D] cache memory

31) A computer system has a 4k word cache organized in block set associative manner with 4 blocks per set , 64 words per block. The number of bits in the SET and WORD fields of the main memory address format is:

2 Marks GATE-CSE/IT-1995( )

[A] 15, 40
[B] 6,4
[C] 7, 2
[D] 4, 6

32) Consider 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively

1 Marks GATE-CSE/IT-2007( )

[A] 9,6,5
[B] 7,7,6
[C] 7,5,8
[D] 9,5,6

33) For inclusion to hold between two cache level L1 and L2 in a multilevel cache hierarchy, which of the following are necessary?

1. L1 must be a write-through cache
2. L2 must be write-through cache
3. The associativity of L2 must be greater that of L1
4. The L2 cache must be at least as large as the L1 cache.

2 Marks GATE-CSE/IT-2008( )

[A] 4 only
[B] and 2 only
[C] 1,2 and 4 only
[D] 1,2,3 and 4

CO Intro

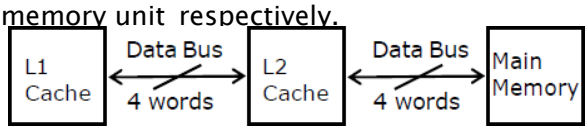
Key Paper

1.	**D**	**2.**	**B**	**3.**	**C**	**4.**	**A**	**5.**	**C**
6.	**C**	**7.**	**B**	**8.**	**A**	**9.**	**B**	**10.**	**A**
11.	**B**	**12.**	**C**	**13.**	**C**	**14.**	**A**	**15.**	**D**
16.	**C**	**17.**	**C**	**18.**	**A**	**19.**	**D**	**20.**	**D**
21.	**A**	**22.**	**C**	**23.**	**C**	**24.**	**D**	**25.**	**B**
26.	**C**	**27.**	**B**	**28.**	**D**	**29.**	**A**	**30.**	**D**
31.	**D**	**32.**	**D**	**33.**	**A**				

Memory interface

Common Data for Q1 and Q2 is given below

A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds. 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively.



1) When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?

2 Marks GATE-CSE/IT-2010,GATE-CSE/IT-2010( )

[A] 2 nanoseconds
[B] 20 nanoseconds
[C] 22 nanoseconds
[D] 88 nanoseconds

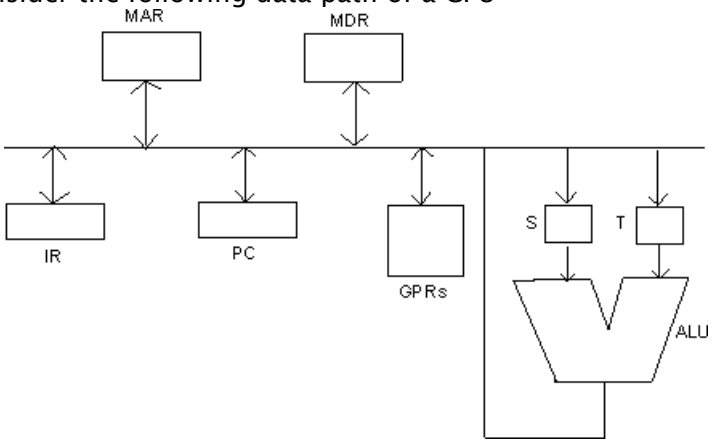
2) When there is a miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers?

2 Marks GATE-CSE/IT-2010( )

[A] 222 nanoseconds
[B] 888 nanoseconds
[C] 902 nanoseconds
[D] 968 nanoseconds

Common Data for Q3 and Q4 is given below

Consider the following data path of a CPU



The, ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycle are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory but into the MDR.

3) The instruction "add R0, R1" has the register transfer in terpretation R0 <= R0 + R1. The minimum number of clock cycles needed for execution cycle of this instruction is

2 Marks GATE-CSE/IT-2005( )

[A] 2
[B] 3
[C] 4
[D] 5

4) The instruction " call Rn, sub " is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is
Rn <= PC + 1 ;
PC <= M [PC];
The minimum number of CPU clock cycles needed during the execution cycle of this instruction is

2 Marks GATE-CSE/IT-2005,GATE-CSE/IT-2005( )

[A] 2
[B] 3
[C] 4
[D] 5

Common Data for Q5 and Q6 is given below

Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3

Instruction	operation	Instruction size (in words)
_MOV R1,5000	; R1 ←Memory [5000]	2
_MOVR2,(R1)	;R2←Memory[(R1)]	1
_ADD R2, R3	; R2 ←R2R3	1
_MOV 6000, R2	;Memory [6000] ←R2	2
HALT	; Machine halts	1

5) Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000(decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address(in decimal saved in the stack will be

2 Marks GATE-CSE/IT-2004( )

[A]1007 [B] 1020

[C]1024 [D]1028

6) Let the clock cycles required for various operations be as follows:

Register to / from memory transfer: 3 clock cycles
ADD with both operands in register: 1 clock cycle
Instruction fetch and decode: 2 clock cycle per word
The total number of clock cycles required to execute the program is

2 Marks GATE-CSE/IT-2004,GATE-CSE/IT-2004( )

[A]29 [B]24

[C]23 [D]20

Common Data for Q7 and Q8 is given below

Consider the following assembly language program for a hypothetical processor. A, B and C are 8 bit registers. The meanings of various instructions are shown as comments.

```
MOV B, # 0          :    B  0
MOV C, # 8          :    C  8Z
CMP C, # 0          :    Compare C with 0
JZX                 :    Jump to X if zero flag is set
SUB C, # 1          :    C C – 1
 RRCA, # 1          :    right rotate A through carry by one bit. Thus :
; if the initial values of A and the carry
 Flag are a7…a0 and
; c0 respectively, their values after the execution of this
 ; instruction will be c0 a7…a1 and a0 respectively.
JCY                 :    Jump to Y if carry flag is set
 JMPZ               :    Jump to ZY
ADDB, # 1           ;    B B + 1
JMPZ                :    Jump to ZX:
```

7) If the initial value of register A is A0, the value of register B after the program execution will be

2 Marks GATE-CSE/IT-2003,GATE-CSE/IT-2003( )

[A] the number of 0 bits in A_0 [B] the number of 1 bits in A0

[C]A_0 [D]8

8) Which of the following instructions when inserted at location X will ensure that the value of register A after program execution is the same as its initial value?

2 Marks GATE-CSE/IT-2003( )

[A] RRCA, # 1 [B] NOP ; no operation

[C]LRCA # 1, ; left rotate A through carry flag by one bit [D]ADDA, # 1

9) Normally user programs are prevented from handling I/O directly by I/O instructions in them. For CPU having explicit I/O instructions, such I/O protection is ensured by having the I/O instructions privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O?

1 Marks GATE-CSE/IT-2005( )

[A] I/O protection is ensured by operating system routine(s) [B] I/O protection is ensured by a hardware trap

[C] I/O protection is ensured during system configuration

[D] I/O protection is not possible

10) A low memory can be connected to 8085 by using

1 Marks GATE-CSE/IT-2001( )

[A] INTER

[B] $\overline{RESET\ IN}$

[C] HOLD

[D] READY

11) Normally user programs are prevented from handling I/O directly by I/O instructions in them. For CPU having explicit I/O instructions, such I/O protection is ensured by having the I/O instructions privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O?

1 Marks GATE-CSE/IT-2005( )

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Memory interface

Key Paper

1.	**D**	**2.**	**D**	**3.**	**C**	**4.**	**B**	**5.**	**C**
6.	**B**	**7.**	**B**	**8.**	**A**	**9.**	**A**	**10.**	**D**
11.	**A**								

Storage manager

Common Data for Q1 and Q2 is given below

A hard disk has 63 sectors per track. 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple $< c, h, s >$ where is the cylinder number, h is the surface number and s is the sector number. Thus, the 0th sector is addressed as $< 0, 0, 0 >$ the 1st sector as $< 0, 0, 1 >$ and so on.

1) The address $< 400, 16, 29 >$ corresponds to sector number :

2 Marks GATE-CSE/IT-2009( )

[A] 505035 [B] 505036
[C] 505037 [D] 505038

2) The address of 1039th sector is

2 Marks GATE-CSE/IT-2009,GATE-CSE/IT-2009( )

[A] $< 0, 15, 31 >$ [B] $< 0, 16, 30 >$
[C] $< 0, 16, 31 >$ [D] $< 0, 17, 31 >$

3) The minimum number of record movements required to merge five files A (with 10 records), B (with 20 records), C (with 15 records), D (with 5 records) and E (with 25 records) is:

2 Marks GATE-CSE/IT-1999( )

[A] 165 [B] 90
[C] 75 [D] 65

4) What is the swap space in the disk used for ?

1 Marks GATE-CSE/IT-2005( )

[A] Saving temporary html pages [B] Saving process data
[C] Storing the super-block [D] Storing device drivers

5) Consider a disk drive with the following specifications. 16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB /sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is

2 Marks GATE-CSE/IT-2005( )

[A] 10 [B] 25
[C] 40 [D] 50

6) Consider a disk pack with 16 surface, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively

1 Marks GATE-CSE/IT-2007( )

[A] 256 Mbyte, 19 bits [B] 256 Mbyte, 28 bits
[C] 512 Mbyte, 20 bits [D] 64 Gbyte, 28 bits

7) For a magnetic disk with concentric circular tracks, the latency is not linearly proportional to the seek distance due to

2 Marks GATE-CSE/IT-2008( )

[A] non-uniform distribution of requests [B] arm starting and stopping inertia
[C] higher capacity of tracks on the periphery of the platter [D] use of unfair arm scheduling policies.

8) What is the swap space in the disk used for ?

1 Marks GATE-CSE/IT-2005( )

[A] Saving temporary html pages [B] Saving process data
[C] Storing the super-block [D] Storing device drivers

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2 Marks GATE-CSE/IT-2005( )

[A] 10 [B] 25
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1 Marks GATE-CSE/IT-2007( )

[A] 256 Mbyte, 19 bits
[B] 256 Mbyte, 28 bits
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[D] 64 Gbyte, 28 bits

11) For a magnetic disk with concentric circular tracks, the latency is not linearly proportional to the seek distance due to

2 Marks GATE-CSE/IT-2008( )

[A] non-uniform distribution of requests
[B] arm starting and stopping inertia
[C] higher capacity of tracks on the periphery of the platter
[D] use of unfair arm scheduling policies.

Storage manager

Key Paper

1.	**C**	**2.**	**C**	**3.**	**A**	**4.**	**B**	**5.**	**B**
6.	**A**	**7.**	**C**	**8.**	**B**	**9.**	**B**	**10.**	**A**
11.	**C**								

Addressing modes

1) Which of the following addressing modes are suitable for program relocation at run time ?
1.Absolute addressing
2. Based addressing
3. Relative addressing 4. Indirect addressing

2 Marks GATE-CSE/IT-2004( )

[A] 1 and 4 [B] 1 and 2
[C] 2 and 3 [D] 1, 2 and 4

2) consider a three word machine instruction
ADD A[R0], @ B
The first operand (destination) " A [R0]" uses indexed addressing mode with R0 as the index register. The second operand(source) "@B" uses indirect addressing mode. A and B are memory address residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction,the two operands are added and stored in the destination (first operand).
The number of memory cycles needed during the execution cycle of the instruction is

2 Marks GATE-CSE/IT-2005( )

[A] 3 [B] 4
[C] 5 [D] 6

3) Match List-I with List-II and select the correct answer using the codes given below the lists :

LIST -I	LIST-II
A. A[1]=B[J];	1. Indirect addressing
B. While[*A++];	2. Indexed addressing
C. int temp = *x;	3. Auto increment

Codes :

2 Marks GATE-CSE/IT-2005( )

	A	B	C		A	B	C
[A]	3	2	1	[B]	1	3	2
[C]	2	3	1	[D]	1	2	3

4) Which of the following is/are true of the auto increment addressing mode ?
1. It is useful in creating self relocating code
2. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation.
3. The amount of increment depends on the size of the data item accessed.

2 Marks GATE-CSE/IT-2008( )

[A] 1 only [B] 2 only
[C] 3 only [D] 2 and 3 only

5) consider a three word machine instruction
ADD A[R_0], @ B
The first operand (destination) " A [R0]" uses indexed addressing mode with R0 as the index register. The second operand(source) "@B" uses indirect addressing mode. A and B are memory address residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).
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2 Marks GATE-CSE/IT-2005( )

[A] 3 [B] 4
[C] 5 [D] 6

6) Match List-I with List-II and select the correct answer using the codes given below the lists

LIST -I	LIST-II
A. A[1]=B[J];	1.Indirect addressing
B. While[*A++];	2.Indexed addressing
C. int temp = *x;	3.Autoincrement

2 Marks GATE-CSE/IT-2005( )

[A]	A-3	B- 2	C-1	[B]	A- 1	B- 3	C-2
[C]	A- 2	B- 3	C-1	[D]	A- 1	B- 2	C-3

Addressing modes

7) Which of the following is/are true of the auto increment addressing mode ?
1. It is useful in creating self relocating code
2. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation.
3. The amount of increment depends on the size of the data item accessed.

2 Marks GATE-CSE/IT-2008( )

[A] 1 only
[B] 2 only
[C] 3 only
[D] 2 and 3 only

8) In the absolute addressing mode

1 Marks GATE-CSE/IT-2002( )

[A] the operand is inside the instruction
[B] the address of the operand is inside the instruction
[C] The register containing the address of the operand is specified inside the instruction
[D] the location of the operand is implicit

9) The main differences(s) between a CSIC and A RISC processor is/are that a RISC processor typically

2 Marks GATE-CSE/IT-1999( )

[A] has fewer instructions
[B] has fewer addressing modes
[C] has more registers
[D] is easier to implement using hard-wired control logic

10) A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor?

2 Marks GATE-CSE/IT-1999( )

[A] Pointers
[B] Pointers
[C] Records
[D] Recursive procedures with local variable

11) Which of the following addressing modes permits relocation without any change whatsoever in the code?

1 Marks GATE-CSE/IT-1998( )

[A] Indirect addressing
[B] Indexed addressing
[C] Base register addressing
[D] PC relative addressing

12) Relative mode of addressing is most relevant to writing

1 Marks GATE-CSE/IT-1996( )

[A] coroutines
[B] position - independent code
[C] shareable code
[D] interrupt handlers

13) A device employing INTR line for device interrupt puts the CALL instruction on the data bus while

1 Marks GATE-CSE/IT-2002( )

[A] $\overline{INTA}$ is active
[B] HOLD is active
[C] READY is active
[D] None of the above

Addressing modes

Key Paper

1.	**C**	**2.**	**D**	**3.**	**C**	**4.**	**C**	**5.**	**D**
6.	**C**	**7.**	**C**	**8.**	**B**	**9.**	**A**	**10.**	**A**
11.	**C**	**12.**	**B**	**13.**	**A**				

DMA

1) A hard disk with a transfer rate of 10M bytes/ second is constantly transferring data to memory using DMA. The processor runs at 600 MHz., and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 K bytes, what is the percentage of processor time consumed for the transfer operations ?

2 Marks GATE-CSE/IT-2004( )

[A] 5.0% [B] 1.0%

[C] 0.5% [D] 0.1%

2) Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line ?

1 Marks GATE-CSE/IT-2005( )

[A] Neither vectored interrupt nor multiple interrupting devices are possible

[B] vectored interrupts are not possible but multiple interrupting devices are possible,

[C] Vectored interrupts and multiple interrupting devices are both possible

[D] Vectored interrupt is possible but multiple interrupting devices are not possible

3) A device with a data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 sec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode ?

2 Marks GATE-CSE/IT-2005( )

[A] 15 [B] 25

[C] 35 [D] 45

4) The use of multiple register windows with overlap causes a reduction in thenumber of memory accesses for

1. function locals and parameters
2. register saves and restores
3. instruction fetches

2 Marks GATE-CSE/IT-2008( )

[A] 1 only [B] 2 only

[C] 3 only [D] 1,2 and 3

5) A CPU generally handles an interrupt by executing an interrupt service routine

1 Marks GATE-CSE/IT-2009( )

[A] as soon as an interrupt is raised

[B] by checking the interrupt register at the end of fetch cycle

[C] by checking the interrupt register after finishing the execution of the current instruction

[D] by checking the interrupt register at fixed time intervals

6) A hard disk with a transfer rate of 10M bytes/ second is constantly transferring data to memory using DMA. The processor runs at 600 MHz., and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 K bytes, what is the percentage of processor time consumed for the transfer operations ?

2 Marks GATE-CSE/IT-2004( )

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[C] 35 [D] 45

DMA

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1. function locals and parameters
2. register saves and restores
3. instruction fetches

2 Marks GATE-CSE/IT-2008( )

[A] 1 only
[B] 2 only
[C] 3 only
[D] 1,2 and 3

10) The correct matching for the following pairs is

(A) DMA I/O	(1) High speed RAM
(B) Cache	(2) Disk
(C) Interrupt I/O	(3) Printer
(D) Condition Code Register	(4) ALU

2 Marks GATE-CSE/IT-1997( )

[A] A – 4 B – 3 C – 1 D – 2
[B] A – 2 B – 1 C – 3 D – 4
[C] A – 4 B – 3 C – 2 D – 1
[D] A – 2 B – 3 C – 4 D – 1

DMA

Key Paper

1.	**D**	**2.**	**B**	**3.**	**B**	**4.**	**A**	**5.**	**C**
6.	**D**	**7.**	**C**	**8.**	**B**	**9.**	**A**	**10.**	**B**

Instruction pipelining

Common Data for Q1 and Q2 is given below

Delayed branching can help in the handling of control hazardous

1) For all delayed conditional branch instructions, irrespective of weather the condition evato true or false, A

2 Marks GATE-CSE/IT-2008( )

[A] the instruction following the conditional branch instruction in memory is executed

[B] the first instruction in the fall through path is executed

[C] the first instruction in the taken path is executed.

[D] the branch takes longer to execute than any other instruction

2) The following code is to run on a pipelined processor with one branch delay slot

11: ADDR2 ← R7 + R8

12: SUB R4 ←R5 – R5x

13 : AD R1 ← R2 + R3

14 : STORE Memory [R4} ← R1

BRANCH to Label if R1= = 0

Which of the instruction 11,12,13 or 14 can legitimately occupy the delay slot without any other program modification ?

2 Marks GATE-CSE/IT-2008,GATE-CSE/IT-2008( )

[A] 11

[B] 12

[C] 13

[D] 14

Common Data for Q4 Q3 and Q5 is given below

Instruction		Operation	Instruction size (no. of words)
MOV	R1, (3000)	R1 ← M[3000]	2
LOOP:			
MOV	R2, R1	R2 ← M[R3]	1
ADD	R2, R1	R2 ← R1 + R2	1
MOV	(R3), R2	M(R3) ← R2	1
INC	R3	R3 ← R3 + 1	1
DEC	R1	R1 ← R1 – 1	1
BNZ	LOOP	Branch on not zero	2
HALT		Stop	

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 100. All the numbers are in decimal.

3) Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

2 Marks GATE-CSE/IT-2007,GATE-CSE/IT-2007,GATE-CSE/IT-2007( )

[A] 10

[B] 11

[C] 20

[D] 21

4) Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is

2 Marks GATE-CSE/IT-2007,GATE-CSE/IT-2007( )

[A] 100

[B] 101

[C] 102

[D] 110

5) Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occur during the execution of the instruction "INC R3", what return address will be pushed on to the stack ?

2 Marks GATE-CSE/IT-2007( )

[A] 1005

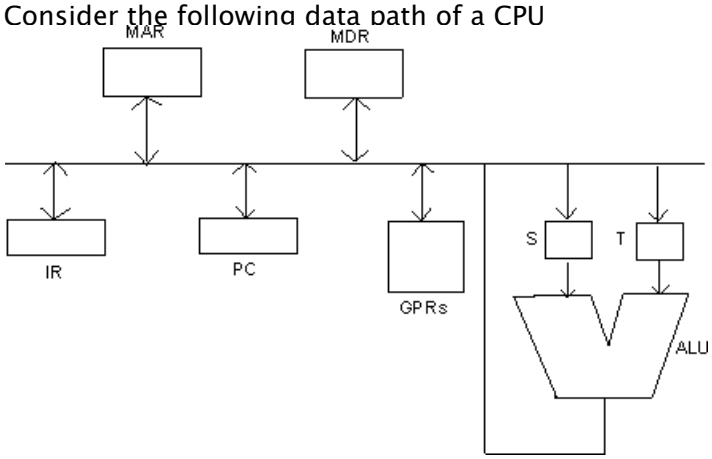
[B] 1020

[C] 1024

[D] 1040

Common Data for Q6 and Q7 is given below

Consider the following data path of a CPU



The, ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycle are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory but into the MDR.

6) The instruction "add R0, R1" has the register transfer in terpretation R0 <= R0 + R1. The minimum number of clock cycles needed for execution cycle of this instruction is

2 Marks GATE-CSE/IT-2005( )

[A] 2 [B] 3
[C] 4 [D] 5

7) The instruction " call Rn, sub "is a two word instruction. Assuming thatPC is incremented during the fetch cycle of the first word of the instruction,its register transfer interpretation is

Rn <= PC + 1 ;
PC <= M [PC];
The minimum number of CPU clockcycles needed during the execution cycle of this instruction is

2 Marks GATE-CSE/IT-2005( )

[A] 2 [B] 3
[C] 4 [D] 5

8) A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each.Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

2 Marks GATE-CSE/IT-2004( )

[A] 120.4 microseconds [B] 160.5 microseconds
[C] 165.5 microseconds [D] 590.0 microseconds

9) A 5 stage pipelined CPU has the following sequence of stages
IF – Instruction fetch from instruction memory.
RD– Instruction decode and register read,
EX– Execute: ALU operation for data and address computation,
MA – Data memory access – for write access the register read at
RD– Stage it used,
WB– Register write backConsider the following sequence of instructions :
I_1: L R0 Locl; R0 <= M[Locl]
I_2 : A R0, R0; R0< = R0 + R0
I_3: A R2, R0; R2< = R2– R0Let each stage take one clock cycle
What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I_1 ?

2 Marks GATE-CSE/IT-2005( )

[A] 8 [B] 10
[C] 12 [D] 15

10) A CPU has 24 – bit instructions. A program starts at address 300(in decimal). Which one of the following is a legal program counter (all values in decimal) ?

2 Marks GATE-CSE/IT-2005( )

[A] 400 [B] 500
[C] 600 [D] 700

11) A CPU has five-stages pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 109 instruction out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, then total execution time of the program is

2 Marks GATE-CSE/IT-2006( )

[A] 1.0second [B] 1.2second
[C] 1.4second [D] 1.6second

12) Consider a pipelined processor with the following four stages
IF : Instruction Fetch
ID: Instruction decode and Operand Fetch
EX: Execute
WB: Write Back
The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction need 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor What is the number of clock cycles taken to complete the following sequence of instructions?.

ADD	R2,	R1,	R0	R2 ← R1+R0
MUL	R4,	R3,	R2	R4 ← R3* R2
SUB	R6,	R5,	R4	R6 ← R5- R4

2 Marks GATE-CSE/IT-2007( )

[A] 7 [B] 8
[C] 10 [D] 14

13) Which of the following are NOT true in a pipelined processor ?
(a) Bypassing can handle all Raw hazards
(b) Register renaming can eliminate all register carried WAR hazards
(c) Control hazard penalties can be eliminated by dynamic branch prediction

2 Marks GATE-CSE/IT-2008( )

[A] 1 and 2 only [B] 1 and 3 only
[C] 2 and 3 only [D] 1,2 and 3

14) In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer)can be accessed is

2 Marks GATE-CSE/IT-2008( )

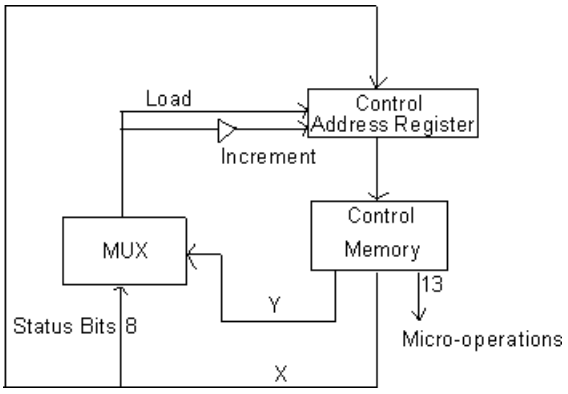
[A] before effective address calculation has started [B] during effective address calculation
[C] after effective address calculation has completed [D] after data cache lookup has completed

15) For a pipelined CPU with a single ALU, consider the following situations
1. The j + 1- st instruction uses the result of the j-th instruction as an operand
2. The execution of a conditional jump instruction
3. The j-th and j + 1-st instructions require the ALU at the same time
Which of the above can cause a hazard ?

1 Marks GATE-CSE/IT-2003( )

[A] 1 and 2 only [B] 2 and 3 only
[C] 3 only [D] All the three

16) The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation filed of 13 bits, a next address field (X), and a MUX select field(Y). There are 8 Status bits in the inputs of the MUX.



How many bits are there in the X and Y fields, and hat is the size of the control memory in number of words ?

2 Marks GATE-CSE/IT-2004( )

[A] 10,3,1024 [B] 8,5,256
[C] 5,8,2048 [D] 10,3,512

17) A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

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MA – Data memory access – for write access the register read at
RD- Stage it used,
WB- Register write back
Consider the following sequence of instructions :
I1 : L R0 Locl; R0 <= M[Locl]
I2 : A R0, R0; R0< = R0 + R0
I3: A R2, R0; R2< = R2- R0
Let each stage take one clock cycle
What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I1 ?

2 Marks GATE-CSE/IT-2005( )

[A] 8 [B] 10
[C] 12 [D] 15

19) A CPU has 24 – bit instructions. A program starts at address 300(in decimal). Which one of the following is a legal program counter (all values in decimal) ?

2 Marks GATE-CSE/IT-2006( )

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20) A CPU has five-stages pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 109 instruction out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, then total execution time of the program is

2 Marks GATE-CSE/IT-2006( )

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21) Consider a pipelined processor with the following four stages
IF : Instruction Fetch
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EX: Execute
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1 Marks GATE-CSE/IT-2007( )

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(b) Register renaming can eliminate all register carried WAR hazards
(c) Control hazard penalties can be eliminated by dynamic branch prediction

2 Marks GATE-CSE/IT-2008( )

[A] 1 and 2 only (b) (c) (c) [B] 1 and 3 only

[C] 2 and 3 only [D] 1,2 and 3

23) Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in
stages S1, S2, S3, S4 is shown below :

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

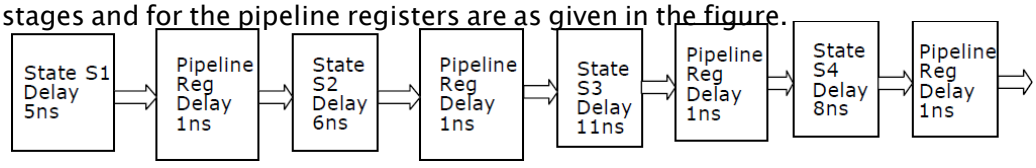
What is the number or cycles needed to execute the following loop ?
For (i=1 to 2) { I1; I2;I3; I4;}

2 Marks GATE-CSE/IT-2009( )

[A] 16 [B] 23

[C] 28 [D] 30

24) Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure.



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

2 Marks GATE-CSE/IT-2011( )

[A] 4.0 [B] 2.5

[C] 1.1 [D] 3.0

25) A micro instruction is to be designed to specify
(a) none or one of the three micro operations of one kind and
(b) none or upto six micro operations of another kind
The minimum number of bits in the micro-instruction is

2 Marks GATE-CSE/IT-1997( )

[A] 9
[B] 5
[C] 8
[D] None of the above

Instruction pipelining

Key Paper

1.	**B**	**2.**	**B**	**3.**	**D**	**4.**	**A**	**5.**	**C**
6.	**B**	**7.**	**B**	**8.**	**C**	**9.**	**B**	**10.**	**C**
11.	**C**	**12.**	**B**	**13.**	**D**	**14.**	**B**	**15.**	**D**
16.	**A**	**17.**	**C**	**18.**	**B**	**19.**	**C**	**20.**	**C**
21.	**B**	**22.**	**D**	**23.**	**B**	**24.**	**B**	**25.**	**C**

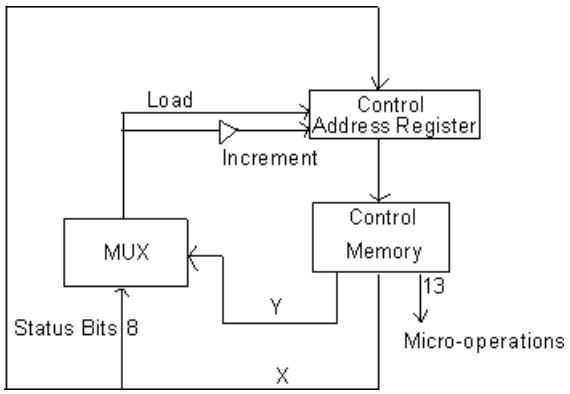
Data & Control modes

1) Consider a new instruction named branch-on-bit-set(mnemonic bbs). The instruction "bbs reg, pos, label" jumps to label if bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.
Temp reg and mask
Branch to label if temp is non-zero
The variable temp is a temporary register. For correct emulation, the variable mask must be generated by

2 Marks GATE-CSE/IT-2006( )

[A] mask <-- Ox1 << pos
[B] mask <-- 0xffffffff >>pos
[C]mask <-- pos
[D]mask <-- 0xf

2) The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro- operation filed of 13 bits, a next address field (X), and a MUX select field(Y). There are 8 Status bits in the inputs of the MUX.



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2 Marks GATE-CSE/IT-2004( )

[A]10,3,1024
[B] 8,5,256
[C]5,8,2048
[D]10,3,512

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Temp ← reg and mask
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The variable temp is a temporary register. For correct emulation, the variable mask must be generated by

2 Marks GATE-CSE/IT-2006( )

[A] mask ← Ox_1 << pos
[B] mask ← 0xffffffff >>pos
[C]mask ← pos
[D]mask ← 0xf

4) Which of the following must be true for the RFE (Return from Exception) instruction on a general purpose processor.
1. It must be a trap instruction
2. It must be a privileged instruction
3. An exception can not be allowed to occur during execution of an RFE instruction

2 Marks GATE-CSE/IT-2008( )

[A]1 only
[B]2 only
[C]1 and 2 only
[D]1, 2 and 3 only

5) Arrange the following configuration for CPU in decreasing order of operating speeds: Hard wired control, vertical microprogramming, horizontal microprogramming.

2 Marks GATE-CSE/IT-1999( )

[A] Hard wired control, vertical micro-programming, horizontal micro- programming.
[B] Hard wired control, horizontal micro-programming, vertical micro- programming.
[C] horizontal micro-programming, vertical micro-programming, Hard wired control.
[D]vertical micro-programming, horizontal micro-programming, hard wired control.

Data & Control modes

6) Which of the following is true?

1 Marks GATE-CSE/IT-1998( )

[A] Unless enabled, a CPU will not be able to process interrupts.

[B] Loop instructions cannot be interrupted till they complete.

[C] A processor checks for interrupts before executing a new instruction.

[D] Only level triggered interrupts are possible on microprocessors

7) The address space of 8086 CPU is

2 Marks GATE-CSE/IT-1998( )

[A] One Megabyte

[B] 256 Kilobytes

[C] 1 K Megabytes

[D] 64 Kilobytes

8) If an instruction takes i microseconds and a page fault takes an additional j microseconds, the effective instruction time if on the average a page fault occurs every k instruction is:

2 Marks GATE-CSE/IT-1998( )

[A] i + j/k

[B] i + j * k

[C] i+j /k

[D] (i+j)*k

9) A micro program control unit is required to generate a total of 25 control signals. Assume that during any microinstruction, at most two control signals are active. Minimum number of bits required in the control word to generate the required control signals will be

2 Marks GATE-CSE/IT-1996( )

[A] 2

[B] 2.5

[C] 10

[D] 12

10) The performance of a pipelined processor suffers if

2 Marks GATE-CSE/IT-2002( )

[A] the pipeline stages have different delays

[B] consecutive instructions are dependent on each other

[C] the pipeline stages share hardware resources

[D] All of the above

Data & Control modes

Key Paper

1.	**A**	**2.**	**A**	**3.**	**A**	**4.**	**D**	**5.**	**B**
6.	**A**	**7.**	**A**	**8.**	**A**	**9.**	**C**	**10.**	**D**